An Efficient VLSI Architecture for Convolution Based DWT Using MAC

Base Paper Abstract:

The modern real time applications related to image processing and etc., demand high performance discrete wavelet transform (DWT). This paper proposes the floating point multiply accumulate circuit (MAC) based 1D/2D-DWT, where the MAC is used to find the outputs of high/low pass FIR filters. The proposed technique is implemented with 45 nm CMOS technology and the results are compared with various existing techniques. The proposed 8 × 8-point floating point 2-levels 2D-DWT achieves 27.6% and 83.7% of reduction in total area and net power respectively as compared with existing DWT.

Enhancement of this project:

- To implement the 2D_DWT(Discrete Wavelet Transform) using Truncation MAC(Multiple Access Accumulator).
- Implement these Technique in VHDL and synthesized in XILINX and shown the comparison table of area, power and delay reports.

Proposed Title:

- **An Efficient and High Performance VLSI Architecture of DWT using Truncation MAC.**

Proposed Abstract:

In functional and numerical analysis , a (DWT) discrete wavelet transform is any wavelet transform for which the wavelets are sampled discretely. In recent research of application of Image Processing there is a demand in high performance and efficient Discrete Wavelet Transform. This paper proposes the new design concept of high performance and efficient Discrete wavelet transform in order to overcome the problem faced in the recent research. The Truncation (MAC) multiply accumulate circuit based on the 2D-DWT is used in the proposed system of this paper, where the high pass and low pass FIR filters output are determined using the MAC. The existing system of DWT uses the concept of Floating point MAC which consumes larger area and its performance was low. Therefore, the proposed technique of DWT using Truncation MAC which achieves a better performance and reduces the area size when compared to existing Floating point MAC concept. The proposed DWT technique with Truncation MAC is implemented in the VHDL and synthesized in the XILINX and compared in terms of area, power and delay reports.

Existing System:

In image processing, DWT can be used in image compression, image reconstruction, image coding, and image fusion. In general, VLSI architecture for DWT is classified into two categories, they are 1) convolution based; and 2) lifting based. Fig. 1 shows the architecture of convolution based DWT with 3 stages, where low pass and high pass filters are represented as H and G respectively. Each filter output samples are decomposed down by the factor of 2. So, at each stage, the number of samples is equal to the half of the previous stage. Here, the input samples are a0, a1,...a7 and the number of input samples is 8. The coefficients of filter G are named as g0, g1, g2, and g3. The coefficients of filter H are h0, h1, h2, and h3. So, the transfer functions of G and H can be written as $G(z)=g0+g1z-1+g2z-2+g3z-3$ and $H(z)=h0+h1z-1+h2z-2+h3z-3$ respectively. The equations (1) and (2) show the high pass and low pass filter outputs in N-point convolution based DWT respectively, where P is the length of the filter and x is input sample. The high pass and low pass filter co-efficients are represented as g and h respectively.

$$yh[k] = P -1\ n=0\ x[-n + 2k].g[n];\ 0 \le k \le N\ 2 - 1\ .....(1)$$

$$yl[k] = P -1\ n=0\ x[-n + 2k].h[n];\ 0 \le k \le N\ 2 - 1.....(2)$$

In Fig. 1, the first stage outputs b and c have 4 samples. The second stage outputs d and e have 2 samples. The last stage outputs f and f have one sample. The high pass outputs are,

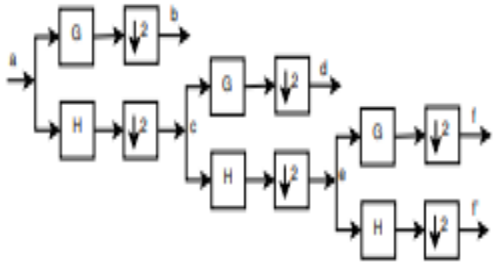


Figure 1: Convolution based 1D DWT with 3 stages

$$\begin{bmatrix} b0 \\ b1 \\ b2 \\ b3 \end{bmatrix} = \begin{bmatrix} a0 & a-1 & a-2 & a-3 \\ a2 & a1 & a0 & a-1 \\ a4 & a3 & a2 & a1 \\ a6 & a5 & a1 & a3 \end{bmatrix} \begin{bmatrix} g0 \\ g1 \\ g2 \\ g3 \end{bmatrix} \text{.....(3)}$$

$$\begin{bmatrix} d0 \\ d1 \end{bmatrix} = \begin{bmatrix} c0 & c-1 & c-2 & c-3 \\ c2 & c1 & c0 & c-1 \end{bmatrix} \begin{bmatrix} g0 \\ g1 \\ g2 \\ g3 \end{bmatrix} \text{.....(4)}$$

$$f0 = g0c0 + g1c - 1 + g2e - 2 + g3e - 3\text{.....(5)}$$

The 2D discrete wavelet transform can be found in 2 steps, they are row process and column process. Here, the input signal sample values are represented as a N × N matrix. During the row process, each row of the input signal matrix is 1D transformed and the results are stored in N × N 2 buffer. After completing all the N rows of input signal matrix, transpose matrix of the buffer is taken for column process. In column process, each row of transposed buffer matrix is 1D transformed and results are the required 2D-transformed values. Fig. 2(a) shows the example for 2D-DWT using 8X8 image signal with 1 level decomposition. Fig. 2(b) shows the example for 2D-DWT with 3 levels of decomposition. Fig. 3(a) and 3(b) show the 1D and 2D folded convolution based DWTs respectively.

Related Works

The following works are found in the VLSI architectures for 1D/2D DWT. The paper [16] shows the VLSI architecture of 2D-DWT. The non-separable convolution based DWTs are shown in [13] [14], where the transpose buffer is not used because the column process is combined with row process.

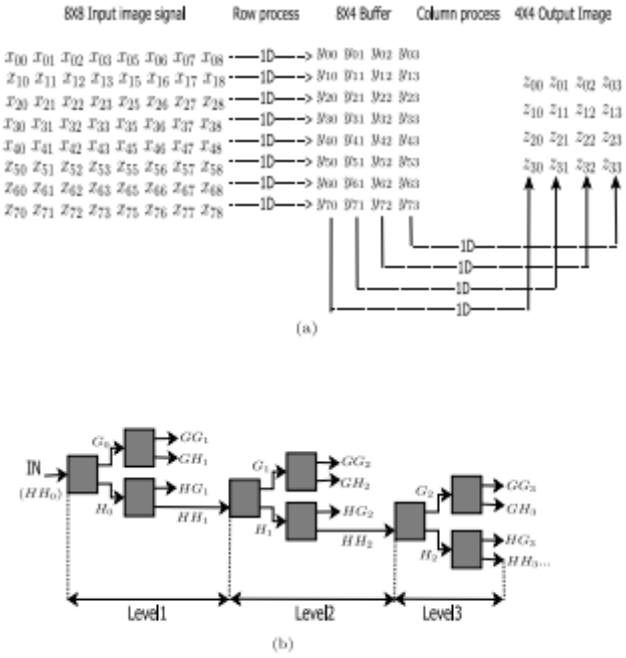


Figure 2: Convolution based 2D-DWT (a) Example: 8X8 image signal with 1 level decomposition and

(b) Example: decomposition with 3 levels

Therefore, multiplication with each filter co-efficient requires two multiplications. The papers [9][10][11] show the convolution based DWTs, where the critical path path involves one multiplier followed by log2b levels of CLA (carry look ahead adder) tree. The multiplier involves log2p levels of CSA (carry save adder) tree and one CLA. Here, b and p are the number of filter co-efficients and number of bits to represent each co-efficient respectively. In [12], separable convolution based 2D-DWT using odd/even decomposition is explained. In [14], non separable parallel convolution based 2D-DWT using the odd/even decomposition is explained. The lifting based parallel architectures are shown in [18][20][22][23], where the transpose buffer is not used and the critical path delay equal to two adders

and one multiplier. The multiply accumulate circuit (MAC) based DWT is shown in [19], where the critical path contains two add-shift based multipliers and four adders. In the folded recursive [17] lifting based DWT, the half of the direct form (9, 7) is used. So, the whole operation takes more cycles to complete as compared with direct form (9, 7) DWT [16]. In the flipping based [25], the co-efficients used in direct form are inverted. In all these lifting based DWT, the drawback is the critical path delay, which increases the energy per operation and decreases the operating frequency.

Disadvantages:

- Low Efficiency
- Consumes Large area.

Proposed system:

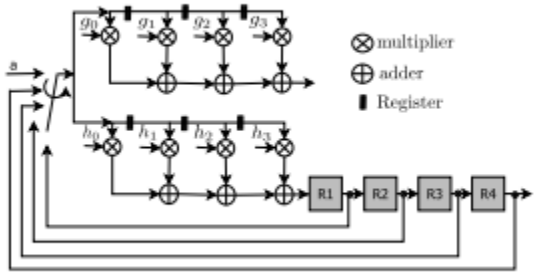
In functional and numerical analysis , a (DWT) discrete wavelet transform is any wavelet transform for which the wavelets are sampled discretely. In recent research of application of Image Processing there is a demand in high performance and efficient Discrete Wavelet Transform. This paper proposes the new design concept of high performance and efficient Discrete wavelet transform in order to overcome the problem faced in the recent research. The Truncation (MAC) multiply accumulate circuit based on the 2D-DWT is used in the proposed system of this paper, where the high pass and low pass FIR filters output are determined using the MAC. The existing system of DWT uses the concept of Floating point MAC which consumes larger area and its performance was low. Therefore, the proposed technique of DWT using Truncation MAC which achieves a better performance and reduces the area size when compared to existing Floating point MAC concept. The proposed DWT technique with Truncation MAC is implemented in the VHDL and synthesized in the XILINX and compared in terms of area, power and delay reports.

The Proposed Convolution Based Floating Point 2d-Dwt Architecture

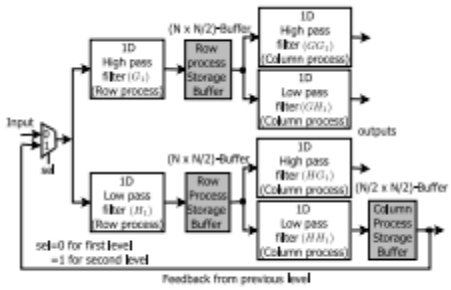
In this section, convolution based floating point 2D-discrete wavelet transform architecture is proposed, which is designed with floating point multiply accumulate circuit (MAC) [21]. The MAC operation can be defined as multiplication and repeated addition. This means that the present multiplication result is added with previous MAC result ($z[j] = z[j-1] + (A[j].B[j])$, where A[j] and B[j] are present input values, z[j] and z[j−1] are present and previous MAC results respectively.

Fig. 4(b) shows proposed 8-point floating point high pass filter (G1) for convolution based 2D-DWT. Here, one stage pipelined floating point MAC is used. If in = 0 then, MAC operations will be performed otherwise multiplication will be performed. The select lines s0 and s1 are used to select the proper inputs based on equations (3) to (5). During the row process of floating point 8×8-input in level 1, the equation (3), requires 12 clock cycles. So, during 1st, 2nd, 5th, and 9th clock cycles of row process in level 1, in = 1 and in = 0 during other clock cycles. Therefore, for each of 12 clock cycles of i th row for 8×8-input matrix of row process in level 1, the corresponding eni = 1 and others are 0 in 8 × 4 buffer as shown in Fig. 4(a). So, totally 96 clock cycles (12 × 8=96) are required to finish the row process of 8 × 8-point input matrix. During the row process of level 2, the equation (4) required 4 clock cycles. Here, in = 1 during 1st and 2nd clock cycles and in = 0 during other clock cycles. So, totally 16 clock cycles (4×4=16) are required to finish the row process. Here, f a0, f a1, and f a2 are the outputs of 4th column of HH1 4 × 4-buffer. If two floating point MACs are used in each filter of Fig. 3(b), then half of the above mentioned clock cycles will be reduced. This way of implementing convolution based floating point 2D-DWT requires less area/power than conventional design, where 4 floating point multipliers and 3 floating point adders are used for each low/high pass filter in row/column processes.

The number of floating point MAC operations in the first level of 1D-DWT is 3b2 4 , where b is the length of low/high pass filters. From the second level onward the number of MAC operations would be b2 4i−1 , where i ≥ 2. The total number of

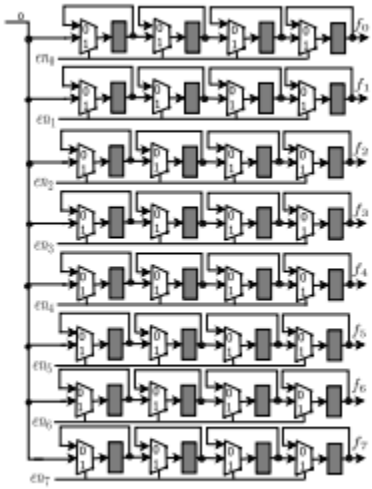


(a)



(b)

Figure 3: (a) Convolution based folded 1D-DWT and (b) The N × N-point convolution based folded 2D-DWT architecture



(a)

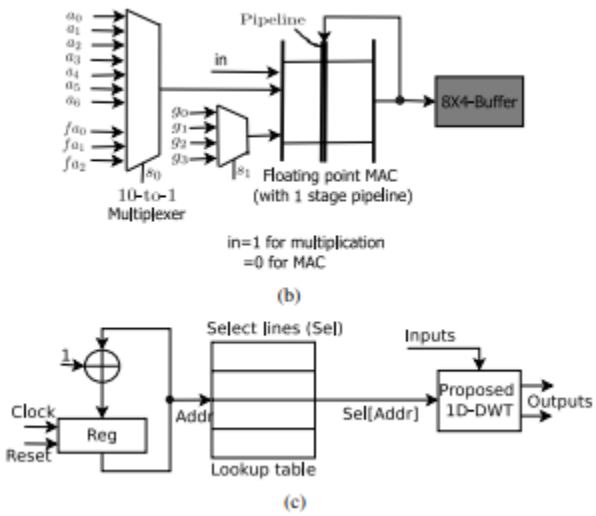


Figure 4: (a) 8 × 4-Buffer used for the row process in proposed floating point convolution based 8 × 8 2D-DWT with 2 levels, (b) Proposed 8-point floating point high pass filter (G1) for convolution based 2D-DWT, and (c) Overall architecture of proposed 1D-DWT for 2D implementation.

floating point MAC operations (number of cycles) (N1D MAC) required for the N-point 1D-DWT with L levels is shown in (6), where N = 2b. Similarly, the total number of floating point MAC operations (number of cycles) (N2D MAC) required for the N × N-point 2D-DWT with L levels is shown in (8), where N = 2b. Here, the number of N-point sequences involved in row and column processes of the first level are N and N 2 respectively. The number of N 2i−1 -point sequences involved in the row and column processes of the i th level are N 2i−1 and N 2.2i−1 respectively, where i ≥ 2.

$$N1D\ MAC\ =\ 3b2\ 4\ +L\ i=2\ b2\ 4i-1 \text{ .....(6)}$$

$$N2D\ MAC\ =\ N\ 3b2\ 4\ +\ N\ 2\ 3b2\ 4\ +L\ i=2\ (\ N\ 2i-1\ +\ N\ 2.2i-1\ )(\ b2\ 4i-1\ ) \text{ .....(7)}$$

$$N2D\ MAC\ =\ 9N\ b2\ 8\ +L\ i=2\ 3N\ b2\ 23i-2 \text{ .....(8)}$$

Advantages:

- High Efficiency.
- Reduces the area size.

Literature Survey:

- Ronald A. DeVore, Bjorn Jawerth and Bradely J. Lucier, “Image Compression Through Wavelet Transform Coding”, IEEE Transactions on Information Theory, 1992, 38 (2), pp. 719-746.-A novel theory is introduced for analyzing image compression methods that are based on compression of wavelet decompositions. This theory precisely relates (a) the rate of decay in the error between the original image and the compressed image as the size of the compressed image representation increases (i.e., as the amount of compression decreases) to (b) the smoothness of the image in certain smoothness classes called Besov spaces. Within this theory, the error incurred by the quantization of wavelet transform coefficients is explained. Several compression algorithms based on piecewise constant approximations are analyzed in some detail. It is shown that, if pictures can be characterized by their membership in the smoothness classes considered, then wavelet-based methods are near-optimal within a larger class of stable transform-based, nonlinear methods of image compression. Based on previous experimental research it is argued that in most instances the error incurred in image compression should be measured in the integral sense instead of the mean-square sense.

- Yong Choi, Ja-Yong Koo, and Nam-Yong Lee, “Image Reconstruction Using the Wavelet Transform for Positron Emission Tomography”, IEEE Transactions on Medical Imaging, 2001, 20 (11), pp. 1188-1193-The authors conducted positron emission tomography (PET) image reconstruction experiments using the wavelet transform. The Wavelet-Vaguelette decomposition was used as a framework from which expressions for the necessary wavelet coefficients might be derived, and then the wavelet shrinkage was applied to the wavelet coefficients for the reconstruction (WVS). The performances of WVS were evaluated and compared with those of the filtered back-projection (FBP) using software phantoms, physical phantoms, and human PET studies. The results demonstrated that WVS gave stable reconstruction over the range of shrinkage parameters and provided better noise and spatial resolution characteristics than FBP.

- Marc Antonini, Michael Barlaud, Pierre Mathieu and Ingrid Daubechies, “Image Coding Using Wavelet Transform”, IEEE Transactions on Image Processing, 1992, 1 (2), pp. 205-220. -A scheme for image compression that takes into account psychovisual features both in the space and frequency domains is proposed. This method involves two steps. First, a wavelet transform used in order to obtain a set of biorthogonal subclasses of images: the original image is decomposed at different scales using a pyramidal algorithm architecture. The decomposition is along the vertical and horizontal directions and maintains constant the number of pixels required to describe the image. Second, according to Shannon's rate distortion theory, the wavelet coefficients are vector quantized using a multiresolution codebook. To encode the wavelet coefficients, a noise shaping bit allocation procedure which assumes that details at high resolution are less visible to the human eye is proposed. In order to allow the receiver to recognize a picture as quickly as possible at minimum cost, a progressive transmission scheme is presented. It is shown that the wavelet transform is particularly well adapted to progressive transmission.

- Jorge Nunez, Xavier Otazu, Octavi Fors, Albert Prades, Vicenc Pala, and Roman Arbiol, “Multiresolution-Based Image Fusion with Additive Wavelet Decomposition”, IEEE Transactions on Geoscience and Remote Sensing, vol. 37, no. 3, pp. 1204-1211, May 1994. -The standard data fusion methods may not be satisfactory to merge a high-resolution panchromatic image and a low-resolution multispectral image because they can distort the spectral characteristics of the multispectral data. The authors developed a technique, based on multiresolution wavelet decomposition, for the merging and data fusion of such images. The method presented consists of adding the wavelet coefficients of the high-resolution image to the multispectral (low-resolution) data. They have studied several possibilities concluding that the method which produces the best results consists in adding the high order coefficients of the wavelet transform of the panchromatic image to the intensity component (defined as L=(R+G+B)/3) of the multispectral image. The method is, thus, an improvement on standard intensity-hue-saturation (IHS or LHS) mergers. They used the "a trous" algorithm which allows the use of a dyadic wavelet to merge nondyadic data in a simple and efficient scheme. They used the method to merge SPOT and LANDSAT/sup TM/ images. The technique presented is clearly better than the IHS and LHS mergers in preserving both spectral and spatial information.

- Nikos D. Zervas, Giorgos P. Anagnostopoulos, Vassilis Spiliotopoulos, Yiannis Andreopoulos, and Costas E. Goutis, “Evaluation of Design Alternatives for the 2-D-Discrete Wavelet Transform”, IEEE Transactions on Circuits and Systems for Video Technology, 2001, 11 (12), pp. 1246- 1262. -In this paper, the three main hardware architectures for the 2-D discrete wavelet transform (2-D-DWT) are reviewed. Also, optimization techniques applicable to all three architectures are described. The main contribution of this work is the quantitative comparison among these design alternatives for the 2-D-DWT. The comparison is performed in terms of memory requirements, throughput, and energy dissipation, and is based on a theoretical analysis of the alternative architectures and schedules. Memory requirements, throughput, and energy are expressed by analytical equations with parameters from both the 2-D-DWT algorithm and the implementation platform. The parameterized equations enable the early but efficient exploration of the various tradeoffs related to the selection to the one or the other architecture.

- Chao-Tsung Huang, Po-Chih Tseng, and Liang-Gee Chen, “Flipping Structure: An Efficient VLSI Architecture for Lifting-Based Discrete Wavelet Transform”, IEEE Transactions on Signal Processing, 2004, 52 (4), pp. 1080-1089. -In this paper, an efficient very large scale integration (VLSI) architecture, called flipping structure, is proposed for the lifting-based discrete wavelet transform. It can provide a variety of hardware implementations to improve and possibly minimize the critical path as well as the memory requirement of the lifting-based discrete wavelet transform by flipping conventional lifting structures. The precision issues are also analyzed. By case studies of the JPEG2000 default lossy (9,7) filter, an integer (9,7) filter, and the (6,10) filter, the efficiency of the proposed flipping structure is demonstrated.

- Si Jung Chang, Moon Ho Lee and Ju Yong Park, “A High Speed VLSI Architecture of Discrete Wavelet Transform for MPEG-4”, IEEE Transactions on Consumer Electronics, 1997, 43 (3), pp. 623-627.-We present a high speed VLSI architecture of the discrete wavelet transform (DWT) for MPEG-4. We found similarities between the computation results of each octave. By using the similarities, in the proposed architecture, the input data are separated between even and odd, and the two data streams are inputted in parallel. This causes faster discrete wavelet transform operation than other architectures. In conventional architectures, the N-point DWT is computed in N cycles or 2N cycles. Whereas, in the proposed architecture the N-point DWT is computed in

N/2 cycles with 100% hardware utilization. Therefore, the proposed architecture can be applied in the MPEG-4 standard, image transmission in wireless networks and digital signal processing which require high speed processing.

- Keshab K. Parhi and Takao Nishitani, "Folded VLSI architectures for discrete wavelet transforms", IEEE International Symposium on Circuits and Systems, May 1993, pp. 1734-1737.- Two classes of novel folded VLSI architectures are presented. They are the word-level folded architecture and the bit-level folded or digit-serial architecture, for implementation of discrete wavelet transforms. In the word-level folded architecture, the computations of all wavelet levels are folded to the same low-pass and high-pass filters. The number of registers in the folded architecture is minimized by the use of generalized life time analysis. The advantage of the word-level folded architecture is low latency, and its drawbacks are increased hardware area, less than 100% hardware utilization, and complex routing and interconnection required by the converters used in this architecture. These drawbacks are eliminated in the alternate bit-level folded digit-serial architecture which requires simpler control circuits, routing, and interconnection, and achieves complete hardware utilization, at the expense of an increase in the system latency and some constraints on the wordlength. In latency-critical applications, the use of the word-level folded architecture is proposed. If latency is not so critical, the use of the bit-level digit-serial architecture is proposed.

- Basant Kumar Mohanty, and Pramod Kumar Meher,"Memory-Efficient High-Speed Convolution-based Generic Structure for Multilevel 2-D DWT", IEEE Transactions on Circuits and Systems for Video Technology, 2013, 23 (2), pp. 353-363. -In this paper, we have proposed a design strategy for the derivation of memory-efficient architecture for multilevel 2-D DWT. Using the proposed design scheme, we have derived a convolution-based generic architecture for the computation of three-level 2-D DWT based on Daubechies (Daub) as well as biorthogonal filters. The proposed structure does not involve frame-buffer. It involves line-buffers of size 3(K -2) M /4 which is independent of throughput-rate, where K is the order of Daubechies/biorthogonal wavelet filter and M is the image height. This is a major advantage when the structure is implemented for higher throughput. The structure has regular data-flow, small cycle period T M and 100% hardware utilization efficiency. As per theoretical estimate, for image size 512 × 512, the proposed structure for Daub-4 filter requires 152 more multipliers and 114 more adders, but

involves 82 412 less memory words and takes 10.5 times less time to compute three-level 2-D DWT than the best of the existing convolution-based folded structures. Similarly, compared with the best of the existing lifting-based folded structures, proposed structure for 9/7-filter involves 93 more multipliers and 166 more adders, but uses 85 317 less memory words and requires 2.625 times less computation time for the same image size. It involves 90 (nearly 47.6%) more multipliers and 118 (nearly 40.1%) more adders, but requires 2723 less memory words than the recently proposed parallel structure and performs the computation in nearly half the time of the other. Inspite of having more arithmetic components than the lifting-based structures, the proposed structure offers significant saving of area and power over the other due to substantial reduction in memory size and smaller clock-period. ASIC synthesis result shows that, the proposed structure for Daub-4 involves 1.7 times less area-delay-product (ADP) and consumes 1.21 times less energy per image (EPI) than the corresponding best available convolution.

References:

[1] Ronald A. DeVore, Bjorn Jawerth and Bradely J. Lucier, “Image Compression Through Wavelet Transform Coding”, IEEE Transactions on Information Theory, 1992, 38 (2), pp. 719-746.

[2] Yong Choi, Ja-Yong Koo, and Nam-Yong Lee, “Image Reconstruction Using the Wavelet Transform for Positron Emission Tomography”, IEEE Transactions on Medical Imaging, 2001, 20 (11), pp. 1188-1193.

[3] Marc Antonini, Michael Barlaud, Pierre Mathieu and Ingrid Daubechies, “Image Coding Using Wavelet Transform”, IEEE Transactions on Image Processing, 1992, 1 (2), pp. 205-220.

[4] Jorge Nunez, Xavier Otazu, Octavi Fors, Albert Prades, Vicenc Pala, and Roman Arbiol, “Multiresolution-Based Image Fusion with Additive Wavelet Decomposition”, IEEE Transactions on Geoscience and Remote Sensing, vol. 37, no. 3, pp. 1204-1211, May 1994.

[5] Nikos D. Zervas, Giorgos P. Anagnostopoulos, Vassilis Spiliotopoulos, Yiannis Andreopoulos, and Costas E. Goutis, “Evaluation of Design Alternatives for the 2-D-Discrete Wavelet Transform”, IEEE Transactions on Circuits and Systems for Video Technology, 2001, 11 (12), pp. 1246- 1262.

[6] Chao-Tsung Huang, Po-Chih Tseng, and Liang-Gee Chen, “Flipping Structure: An Efficient VLSI Architecture for Lifting-Based Discrete Wavelet Transform”, IEEE Transactions on Signal Processing, 2004, 52 (4), pp. 1080-1089.

[7] Si Jung Chang, Moon Ho Lee and Ju Yong Park, “A High Speed VLSI Architecture of Discrete Wavelet Transform for MPEG-4”, IEEE Transactions on Consumer Electronics, 1997, 43 (3), pp. 623-627.

[8] Keshab K. Parhi and Takao Nishitani, “Folded VLSI architectures for discrete wavelet transforms”, IEEE International Symposium on Circuits and Systems, May 1993, pp. 1734-1737.

[9] Basant Kumar Mohanty, and Pramod Kumar Meher,“Memory-Efficient High-Speed Convolution-based Generic Structure for Multilevel 2-D DWT”, IEEE Transactions on Circuits and Systems for Video Technology, 2013, 23 (2), pp. 353-363.

[10] Chaitali Chakrabarti, and Mohan Vishwanath, “Efficient Realizations of the Discrete and Continuous Wavelet Transforms: From Single Chip Implementations to Mappings on SIMD Array Computers”, IEEE Transactions on Signal Processing, 1995, 43 (3), pp. 759-771.

[11] Pramod Kumar Meher, Basant Kumar Mohanty, and Jagdish Chandra Patra, “Hardware-Efficient Systolic-Like Modular Design for TwoDimensional Discrete Wavelet Transform”, IEEE Transactions on Circuits and Systems - II, 2008, 55 (2), pp. 151-155.

[12] Po-Cheng Wu and Liang-Gee Chen, “An Efficient Architecture for Two-Dimensional Discrete Wavelet Transform”, IEEE Transactions on Circuits and Systems for Video Technology, 2001, 11 (4), 536-545.

[13] Chu Yu and Sao-Jie Chen, “VLSI Implementation of 2-D Discrete Wavelet Transform for Real-time Video Signal Processing”, IEEE Transactions on Consumer Electronics, 1997, 43 (4), pp. 1270-1279.

[14] Francescomaria Marino, “Efficient High-Speed/Low-Power Pipelined Architecture for the Direct 2-D Discrete Wavelet Transform”, IEEE Transactions on Circuits and Systems - II: Analog and Digital Signal Processing, 2000, 47 (12), pp. 1476-1491.

[15] Tinku Acharya and Chaitali Chakrabarti, “A Survey on Lifting-based Discrete Wavelet Transform Architectures”, Journal of VLSI Signal Processing, 2005, 42, pp. 321-339.

[16] Liu Hong-jin, Shao Yang, He Xing, Zhang Tie-jun, Wang Dong-hui and Hou Chao-huan, “A Novel VLSI Architecture for 2-D Discrete Wavelet Transform”, IEEE International Conference on ASIC, Oct. 2007, pp. 40-43.

[17] Guangming Shi, Weifeng Liu, Li Zhang, and Fu Lii, “An Efficient Folded Architecture for Lifting-Based Discrete Wavelet Transform”, IEEE Transactions on Circuits and Systems-II: Express Briefs, 2009, 56 (4), pp. 290-294.

[18] Chengyi Xiong, Jinwen Tian, and Jian Liu, “Efficient Architectures for Two-Dimensional Discrete Wavelet Transform Using Lifting Scheme”, IEEE Transactions on Image Processing, 2007, 16 (3), pp. 607-614.

[19] Chih-Hsien Hsia, Jen-Shiun Chiang, Member, and Jing-Ming Guo, “Memory-Efficient Hardware Architecture of 2-D Dual-Mode LiftingBased Discrete Wavelet Transform”, IEEE Transactions on Circuits and Systems for Video Technology, 2013, 23 (4), pp. 671-683.

[20] Xin Tian, Lin Wu, Yi-Hua Tan, and Jin-Wen Tian, “Efficient MultiInput/Multi-Output VLSI Architecture for Two-Dimensional LiftingBased Discrete Wavelet Transform”, IEEE Transactions on Computers, 2011, 60 (8), pp. 1207-1211.

[21] Mohamed Asan Basiri M and Noor Mahammad Sk, “An efficient Hardware Based Higher Radix Floating Point MAC Design”, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2014, 20 (1), pp. 15:1-15:25.

[22] Wei Zhang, Zhe Jiang, Zhiyu Gao, and Yanyan Liu, “An Efficient VLSI Architecture for Lifting-Based Discrete Wavelet Transform”, IEEE Transactions on Circuits and Systems-II: Express Briefs, 2012, 59 (3), pp. 158-162, Mar. 2012.

[23] Basant K. Mohanty, Anurag Mahajan, and Pramod K. Meher, “Areaand Power-Efficient Architecture for High-Throughput Implementation of Lifting 2-D DWT”, IEEE Transactions on Circuits and Systems-II: Express Briefs, 2012, 59 (7), pp. 434-438.

[24] Boon Hui Ang, Usman Ullah Sheikh, and Muhammad Nadzir Marsono, “2-D DWT System Architecture for Image Compression”, Journal of Signal Processing Systems, Springer, 2015, (78), pp. 131-137.

[25] Anand Darji, Member, Shubham Agrawal, Ankit Oza, Vipul Sinha, Aditya Verma, S. N. Merchant, and A. N. Chandorkar, “Dual-Scan Parallel Flipping Architecture for a Lifting-Based 2-D Discrete Wavelet Transform”, IEEE Transactions on Circuits and Systems-II: Express Briefs, 2014, 61(6), pp. 433-437.

[26] Hanaa ZainEldin, Mostafa A. Elhosseini, Hesham A. Ali, “Image compression algorithms in wireless multimedia sensor networks: A survey”, Ain Shams Engineering Journal, Elsevier, 2015 (6), pp. 481-490.

[27] Tatsuya Murofushi, Toshiyuki Dobashi, Masahiro Iwahashi, and Hitoshi Kiya, “An Integer Tone Mapping Operation for HDR Images in Openexr With Denormalized Numbers”, IEEE International Conference on Image Processing (ICIP), (2014) 4497-4501.